

L Number	Hits	Search Text	DB	Time stamp
1	1441	hsiao.in. or lo-hao-liang.in. or yang-li-yang.in.	USPAT; US-PGPUB; EPO	2003/09/11 12:51
2	1	hsiao-k\$-t\$.in. or lo-hao-liang.in. or yang-li-yang.in.	USPAT; US-PGPUB; EPO	2003/09/11 12:53
3	1	hsiao-k\$-t\$.in. or lo-hao-liang.in. or yang-li-yang.in.	USPAT; US-PGPUB; EPO	2003/09/11 12:53
4	1	hsiao-k\$-t\$.in. or lo-hao-liang.in. or yang-li-yang.in.	USPAT; US-PGPUB; EPO; JPO	2003/09/11 12:53
5	1	hsiao-k\$-t\$.in. or lo-hao-liang.in. or yang-li-yang.in.	USPAT; US-PGPUB; EPO; JPO	2003/09/11 13:26
6	8375	microprocess\$4 and clock\$2 adj signal\$2 and output\$2 and input\$2 and memory and stor\$4 and test\$4 and compar\$5	USPAT; US-PGPUB; EPO; JPO	2003/09/11 13:31
7	0	microprocess\$4 and clock\$2 adj signal\$2 and output\$2 and input\$2 and memory and stor\$4 and test\$4 and compar\$5 and 714.ccls.	USPAT; US-PGPUB; EPO; JPO	2003/09/11 13:32
8	869	microprocess\$4 and clock\$2 adj signal\$2 and output\$2 and input\$2 and memory and stor\$4 and test\$4 and compar\$5 and 714/\$.ccls.	USPAT; US-PGPUB; EPO; JPO	2003/09/11 13:32
9	281	microprocess\$4 and clock\$2 adj signal\$2 and output\$2 and input\$2 and memory and stor\$4 and test\$4 and compar\$5 and 714/\$.ccls. and CPU and buffer	USPAT; US-PGPUB; EPO; JPO	2003/09/11 13:33
10	1	microprocess\$4 and clock\$2 adj signal\$2 and output\$2 and input\$2 and memory and stor\$4 and test\$4 and compar\$5 and 714/\$.ccls. and CPU and buffer and hardware adj time adj delay	USPAT; US-PGPUB; EPO; JPO	2003/09/11 13:34
11	1	microprocess\$4 and clock\$2 adj signal\$2 and output\$2 and input\$2 and memory and stor\$4 and test\$4 and compar\$5 and CPU and buffer and hardware adj time adj delay	USPAT; US-PGPUB; EPO; JPO	2003/09/11 13:34
12	374	microprocess\$4 and clock\$2 adj signal\$2 and output\$2 and input\$2 and memory and stor\$4 and test\$4 and compar\$5 and CPU and buffer and hardware and time adj delay	USPAT; US-PGPUB; EPO; JPO	2003/09/11 13:35
13	386	microprocess\$4 and clock\$2 adj signal\$2 and output\$2 and input\$2 and memory and stor\$4 and test\$4 and compar\$5 and CPU and buffer\$ and hardware and time adj delay	USPAT; US-PGPUB; EPO; JPO	2003/09/11 13:37
14	386	microprocess\$4 and clock\$2 adj signal\$2 and output\$2 and input\$2 and memory and stor\$4 and test\$4 and compar\$5 and CPU and buffer\$ and hardware and time adj delay and py<2001	USPAT; US-PGPUB; EPO; JPO	2003/09/11 13:38
15	255	microprocess\$4 and clock\$2 adj signal\$2 and output\$2 and input\$2 and memory and stor\$4 and test\$4 and compar\$5 and CPU and buffer\$ and hardware and time adj delay and @py<2001	USPAT; US-PGPUB; EPO; JPO	2003/09/11 13:39
16	386	microprocess\$4 and clock\$2 adj signal\$2 and output\$2 and input\$2 and memory and stor\$4 and test\$4 and compar\$5 and CPU and buffer\$ and hardware and time adj delay and @py<20010628	USPAT; US-PGPUB; EPO; JPO	2003/09/11 13:40
17	386	microprocess\$4 and clock\$2 adj signal\$2 and output\$2 and input\$2 and memory and stor\$4 and test\$4 and compar\$5 and CPU and buffer\$ and hardware and time adj delay and @py<20000628	USPAT; US-PGPUB; EPO; JPO	2003/09/11 13:40

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18	(217)	microprocess\$4 and clock\$2 adj signal\$2 and output\$2 and input\$2 and memory and stor\$4 and test\$4 and compar\$5 and CPU and buffer\$ and hardware and time adj delay and @py<2000	USPAT; US-PGPUB; EPO; JPO	2003/09/11 13:40
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